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Comparison between Conventional and Modified Cascaded H-Bridge Multilevel Inverter-Fed Drive

Gleena Varghese[1], Tissa Tom[2], Jithin K Sajeev[3]

PG Student, Dept. of Electrical and Electronics Engg., St.Joseph's College of Engg., and Technology, Palai, India[1]

Assistant Professor, Dept. of Electrical & Electronics Engg., St.Joseph's College of Engg., & Technology, Palai, India[2]

Assistant Professor, Department of Electrical and Electronics Engineering , College of Engineering , Idukki, India[3]

Abstract: Inverters are static power electronics devices which convert dc input voltage to ac output voltage with the desired magnitude and frequency. The output voltage waveforms of ideal inverters should be sinusoidal. But practically it is square-wave or quasi-square-wave. To get better waveforms with low harmonic distortion, multi- level inverters are used. Multilevel inverter starts with a level of three. The topology used here is cascaded H-Bridge and the modulation technique is sinusoidal pulse width modulation. Here a comparison between conventional and modified cascaded H-Bridge inverter is done. The load of the inverter is induction motor. The number of output voltage level is five. Simulation is done in MATLAB 2011b environment and the waveforms are obtained. Finally, a prototype circuit of modified Cascaded H-Bridge inverter is implemented.. The results are analyzed using MATLAB/SIMULINK software. The hardware implementation is done using FPGA.

Keywords: Sinusoidal Pulse Width Modulation, Cascaded H-Bridge, Total Harmonic Distortion, FPGA.

I. INTRODUCTION

The most common initial application of multilevel converters has been in traction, both in locomotives and trackside static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high voltage dc transmission, and most recently for medium voltage induction motor variable speed drives. Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems.

The concept of multilevel converters has been introduced since 1975. The name of multilevel can start with a voltage level of three. There are mainly three topologies for multilevel inverters. They are Diode clamped multilevel inverters, flying capacitor multilevel inverters and cascaded H-bridge multilevel inverter.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM).

The attractive features of a multilevel converter can be briefly summarized as follows [2] :

- Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
- Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies.
- Input current: Multilevel converters can draw input current with low distortion.
- Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.
- Increased number of voltage levels which leads to better voltage waveforms.
- Reduced switching stresses on the devices due to the reduction of step voltages between the levels.

The cascade multilevel inverter was first proposed in 1975. In cascaded H-bridge topology, separate DC-sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage [1]. The Cascaded H-bridge topology has many advantages than the other two topologies. It requires the least number of components among all multilevel converters and also the regulation of dc buses is simple.

The rest of the paper is organized as follows:

The topology of conventional and modified cascaded H-bridge multilevel inverter and then explains the modulation technique used. Then the conclusion is obtained from the simulation results and experimental results. The hardware implementation is done using FPGA..

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II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Fig. 1 shows the circuit diagram of cascaded H-bridge multilevel inverter. The concept of this inverter is based on connecting H-bridge inverters in series. The outputs of the H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The dc link supply for each full bridge inverter is provided separately, and this is typically achieved using diode rectifiers without using the single-phase transformer. The converter topology is based on the series connection of single-phase inverters with separate dc sources the resulting phase voltage is synthesized by the addition of the voltages generated by the different cells.

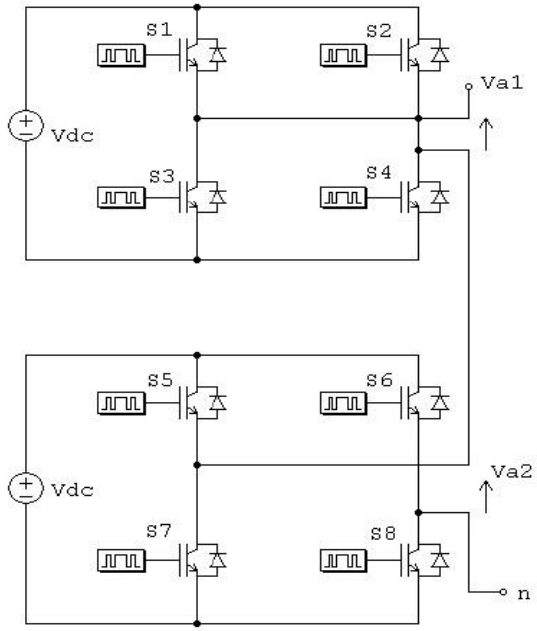

Fig.1. Cascaded H-Bridge Multilevel Inverter

The switching sequence of cascaded H-bridge topology is shown in Table I. The number of output voltage levels is 2n+1, where n is the number of cells. Here the output voltage levels are +2V, +V, 0, -V and -2V. When the switches S_1, S_4, S_5 and S_8 are turned on, the output voltage is +2V. When the switches S_2, S_3, S_6 and S_7 are turned on, the output voltage is -2V. Similarly switching is done for other voltage levels also.

The output voltage is, $V_o = V_1 + V_2$

Output Voltage V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_5=2V_{dc}$	1	0	0	1	1	0	0	1
$V_4=V_{dc}$	1	0	0	1	1	1	0	0
$V_3=0$	1	1	0	0	1	1	0	0
$V_2=-V_{dc}$	1	1	0	0	0	1	1	0
$V_1=-2V_{dc}$	0	1	1	0	0	1	1	0

TABLE I: Switching Sequence of Cascaded H-Bridge Multilevel Inverter

III. MODIFIED CASCADED H-BRIDGE MULTILEVEL INVERTER

Fig. 2 shows the circuit diagram of modified cascaded H-bridge multilevel inverter. The power circuit of modified cascaded multilevel inverter is such that it can produce more output levels with reduced number of power switches. It uses only 5 switches to get an output voltage of five level whereas conventional cascaded inverter uses 8 switches. The modified five level cascaded H-bridge MLI using one H-bridge and one power semiconductor switch as shown in Fig. Here only one dc source is used and then it is divided by using a dc bus capacitor. Therefore, less number of components are used to generate the five level output voltage [3].

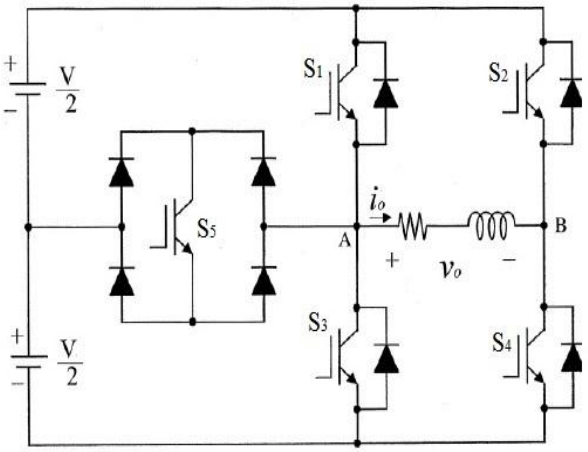

Fig. 2: Modified Cascaded H-Bridge Multilevel Inverter

The switching pattern of modified cascaded inverter is shown in Table II. The output voltage levels are V, V/2, 0, -V/2 and –V.

Output Voltage	S_1	S_2	S_3	S_4	S_5
V	1	0	0	1	0
V/2	0	0	0	1	1
0	0	0	1	1	0
-V/2	0	1	0	0	1
-V	0	1	1	0	0

TABLE II: Switching Sequence of Modified Cascaded H- Multilevel Inverter

IV. SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE

In Sinusoidal Pulse Width Modulation (SPWM) technique the signal is generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c [1]. The frequency of the reference signal is f_r determines the output frequency f_o and its peak amplitude is A_r controls the modulation index M. The gating signal for SPWM technique is shown in Fig. 3.

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The output waveforms are given in the form of pulses by comparing the reference and carrier signals [3].

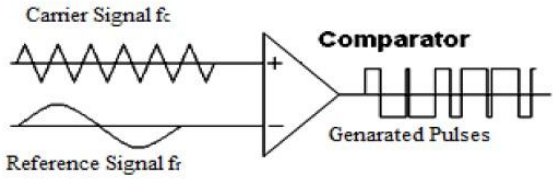

Fig. 3 Principle of PWM Generation

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge inverters. Total harmonics distortion of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation. An m-level multilevel inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude.

In level-shifted modulation, in phase disposition method is used. In this method all the carriers are in phase. If the voltage level N is 5, there will be N-1 number of carrier waveforms. Fig. 4 shows the level shifted in phase disposition PWM method [5][6].

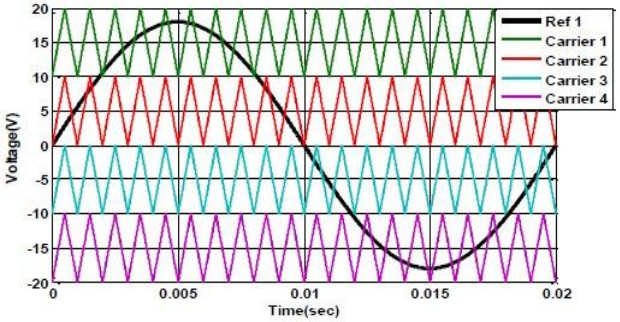

Fig. 4: In Phase Disposition

V. SIMULATION RESULTS

The simulation of conventional cascaded and modified cascaded multilevel inverter is done using MATLAB/SIMULINK.

A. Cascaded H-bridge Multilevel Inverter

Fig. 5 shows the output pulses for the switches S_1-S_8

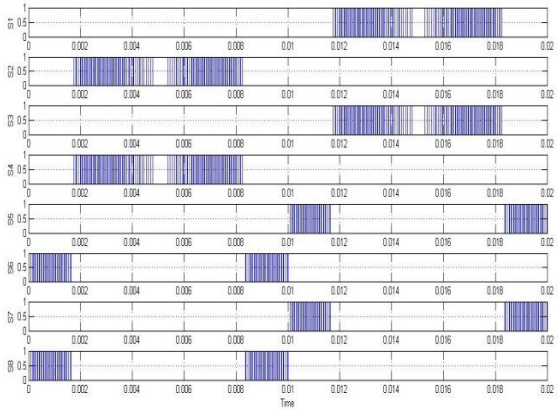

Fig. 5: Switching Pulses for Cascaded H-Bridge MLI

Fig. 6 shows the three phase output voltage of conventional cascaded H-bridge multilevel inverter. The simulation is done at a modulation index of 1and the input voltage is 120 V.

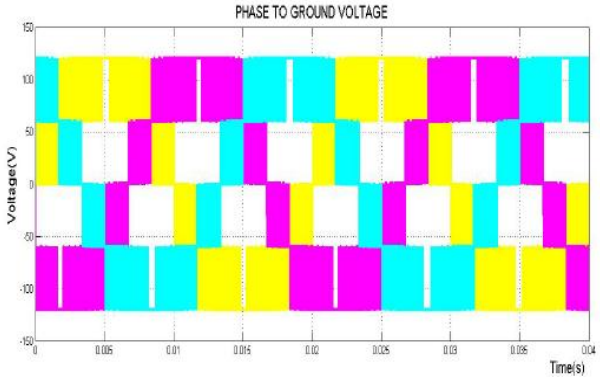

Fig. 6: Output Voltage of Cascaded H-Bridge MLI

The peak to peak voltage is 240 V. The stator current and speed response of conventional inverter-fed drive is shown in Fig. 7 and Fig. 8. Speed is found to be 255 RPM.

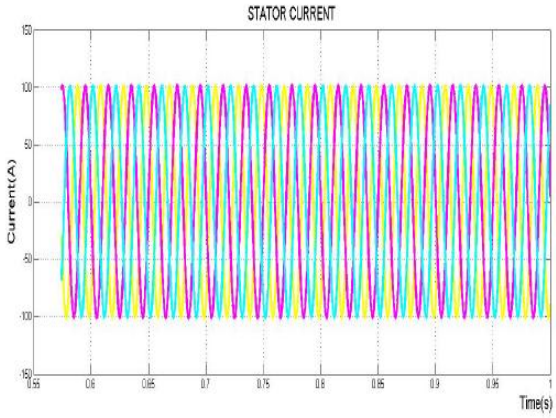

Fig. 7: Stator Current of Conventional Inverter-Fed Drive

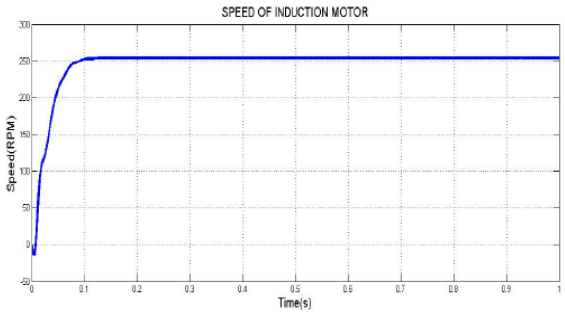

Fig. 8: Speed Response of Conventional Inverter-Fed Drive

B. Modified Cascaded H-bridge Multilevel Inverter

Fig. 9 shows the output pulses for the switches S_1-S_5 and the Fig. 10 shows the output voltage of modified cascaded H-bridge multilevel inverter. The simulation is done at a modulation index of 1. The input voltage is 120 V.

The peak to peak voltage is 240 V. The stator current and speed response of modified inverter-fed drive is shown in Fig. 11 and Fig. 12. Speed is found to be 255 RPM.

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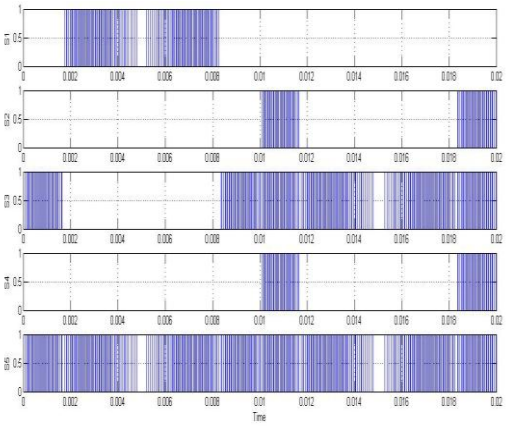

Fig. 9: Switching Pulses for Modified Cascaded H-Bridge MLI

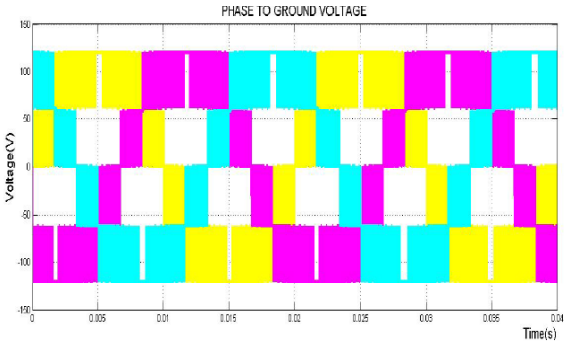

Fig. 10: Output Voltage of Modified Cascaded H-Bridge MLI

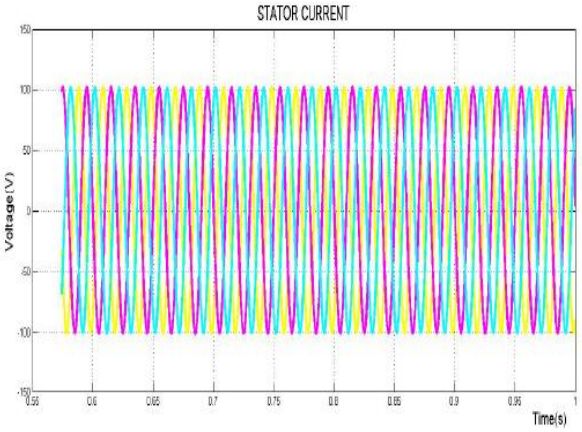

Fig. 11: Stator Current of Conventional Inverter-Fed Drive

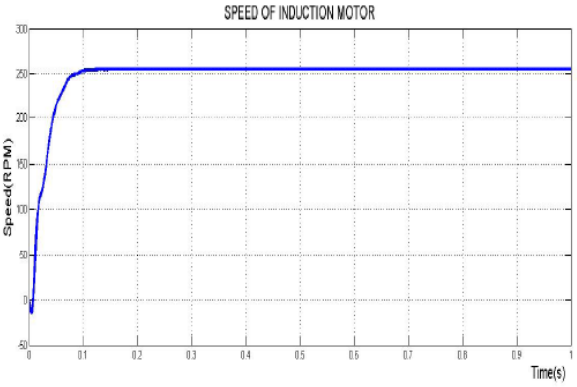

Fig. 12: Speed Response of Inverter-Fed Drive

C. Comparison Between Conventional and Modified Cascaded Inverter

The harmonic spectrum of conventional cascaded H-bridge multilevel inverter is shown in Fig. 13. The value of THD is 26.78%.

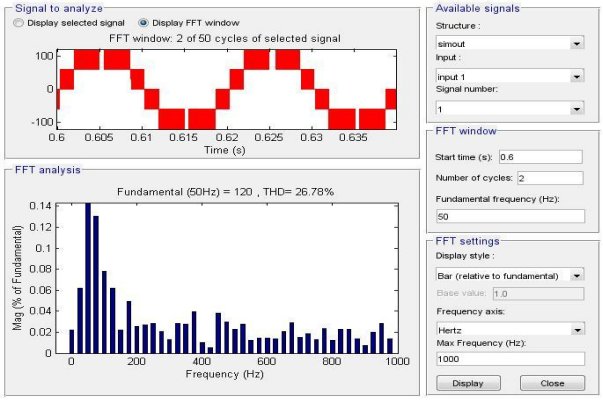

Fig. 13: Harmonic Spectrum of Conventional Cascaded H-Bridge MLI

The harmonic spectrum of modified cascaded H-bridge multilevel inverter is shown in Fig. 14. The THD value is 26.26%.

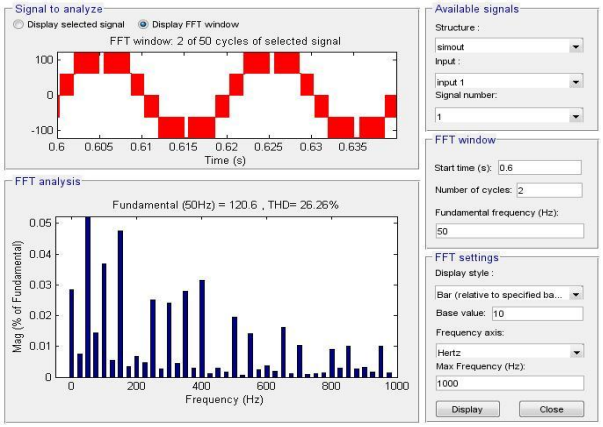

Fig. 14: Harmonic Spectrum of Modified Cascaded H-Bridge MLI

The harmonic spectrum of stator current of conventional inverter-fed drive and modified inverter-fed drive are shown in Fig. 15 and Fig. 16. The values are 0.37% and 0.81% respectively.

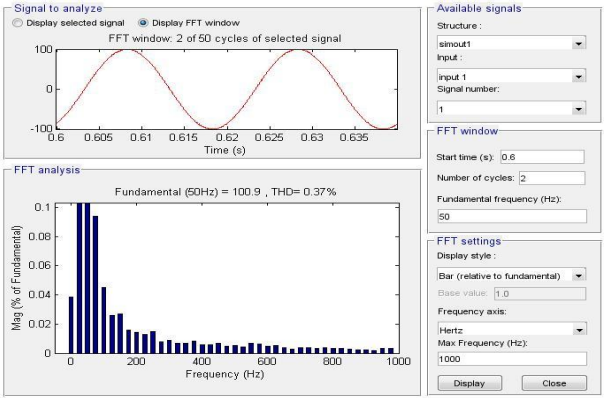

Fig. 15: Harmonic Spectrum of Stator Current of Conventional Inverter - Fed Drive

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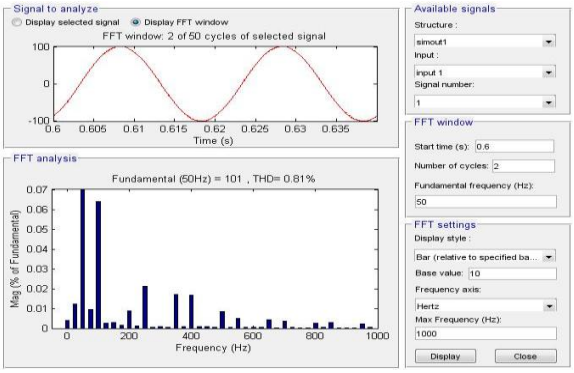

Fig. 16: Harmonic Spectrum of Stator Current of Modified Inverter - Fed Drive

The THD of output voltage of modified inverter is less than the conventional cascaded H-bridge multilevel inverter. But the THD of stator current conventional inverter-fed drive is less than the modified one. The speed response of the two drives is almost similar. An advantage of modified cascaded inverter is that it needs only five switches to produce five level output voltage whereas eight switches are needed in conventional cascaded inverter for the same. This reduces the circuit complexity, cost and weight.

VI. EXPERIMENTAL SETUP

Fig. 17 shows the main circuit of the hardware set up of modified cascaded-H-Bridge inverter-fed drive.

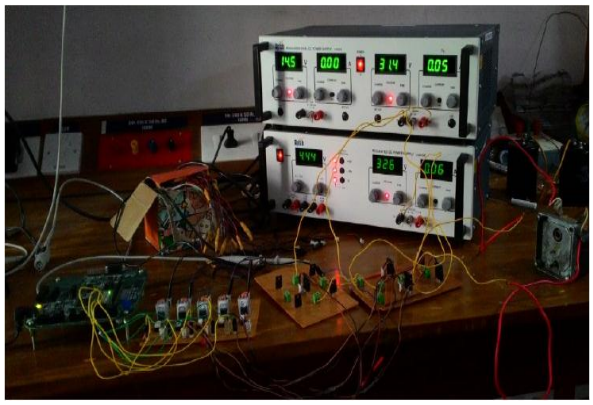

Fig. 17: Hardware Setup of Modified Inverter-Fed Drive

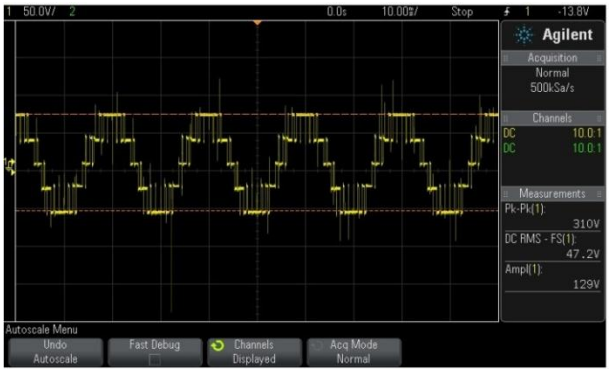

Fig. 18: Output Waveform of Modified Inverter-Fed Drive

The control signals are given to the switches using FPGA (Field Programmable Gate Array)and the driver IC is TLP250. The load of the inverter is induction motor of rating 230 V, 190 W. The input dc voltage applied is 60 V. The output waveform of modified inverter while driving an induction motor is shown in Fig. 18 and the speed of the motor is found to be 150 RPM using tachometer.

VII. CONCLUSION

The simulation of two topologies is done using MATLAB/SIMULINK and the hardware implementation of modified inverter-fed drive is done using FPGA. From the comparison of two topologies, modified cascaded multilevel inverter is found to better than the conventional one. It has got many advantages like reduced number of switches, low harmonic distortion of output voltage for higher switching frequencies, the circuit complexity is reduced, low cost and weight.

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